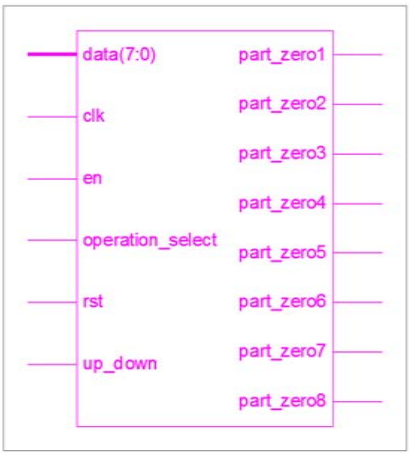


Figure : Top Partition

2. Hash function

The hash function is used to enter/delete an item into/from a list. When an item is checked weather it is in a particular list the answer may be a false positive. The false positiveness will be reduced by hash function. The input data is 8 bit and it has 8 single bit outputs.

3. Partitions

The addresses of the item to be entered into the list or deleted from the list or searched weather it is in the list or not is decoded and given to the 8 individual partitions. The each partition has a single bit output.

4. Gated clock

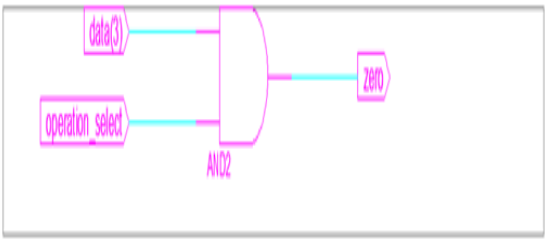


Figure: Gated Clock

The gated clock is an unit that has two inputs and output. One input is 4 bit input data and the other is the type of operation to be performed.

SIMULATION RESULTS

Simulation is a powerful and important tool because it provides a way in which alternative designs, plans and/or policies can be evaluated without having to experiment on a real system, which may be prohibitively costly, time consuming, or simply impractical to do.

1. Generating Hash function

The hash function is used to enter/delete an item into/from a list. When an item is checked weather it is in a particular list the answer may be a false positive. The false positiveness will be reduced by hash function. The input data is 8 bit and it has 8 single bit outputs.

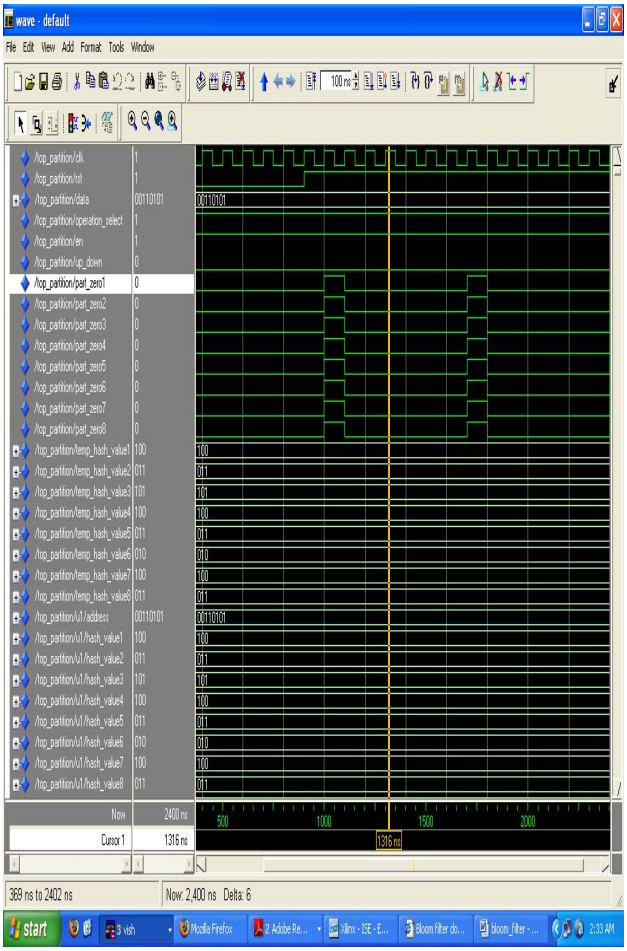


Figure : Generating hash function

2. Individual Partition

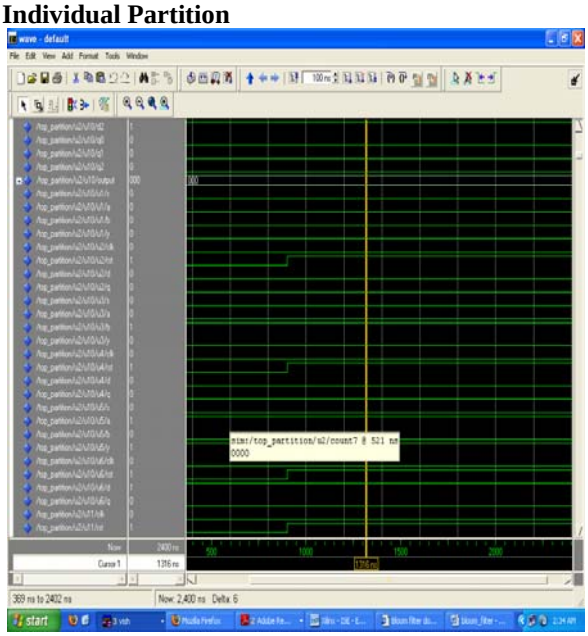
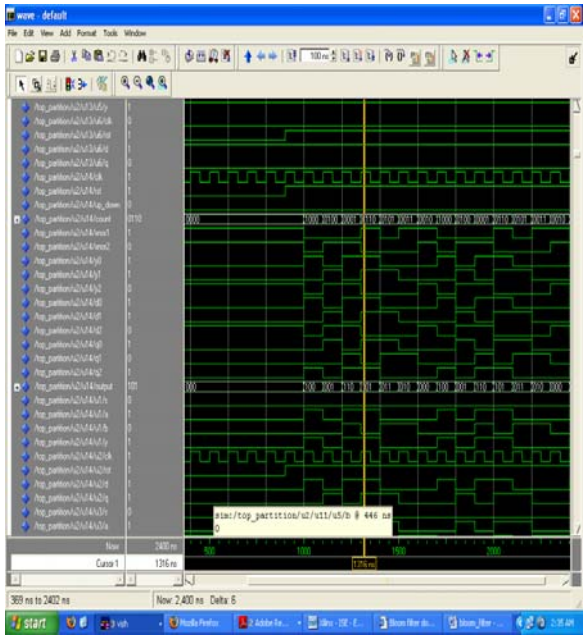


Figure : Individual partition result

The address of the item to be enter into the list or deleted from the list or searched weather it is in the list or not is decoded and given to the 8 individual partitions. The each partition has a single bit output. The output of the partition is either 1 or 0 based on whether the particular item is in the list or not.

3. LFSR Count



The LFSR's are used in up/down counters. When an item enters into a list its count increased by 1.if an item deleted from a set then the count will be decreased by 1. An LFSR is a shift register that, when clocked, advances the signal through the register from one bit to the next most-significant bit . Some of the outputs are combined in exclusive OR configuration to form a feedback mechanism. A linear feedback shift register can be formed by performing exclusive OR on the outputs of two or more of the flip-flops together and feeding those outputs back into the input of one of the flip-flops.

CONCLUSION

In this thesis the investigation of physical level implementations of CBFs is done and proposed LCBF. LCBF is a novel implementation consisting of an array of up/down LFSRs and zero detectors. Compare LCBF with SCBF is made. SCBF is the previously assumed implementation consisting of an SRAM array of counts and a shared counter. LCBF is superior to SCBF in both delay and speed at the expense of more area. The proposed LCBF is a novel implementation consisting of an array of up/down LFSRs and zero detectors. It will test the membership of the set by Increment, Decrement and probe operations in LFSR .It will produce the single out "is zero". Comparisons demonstrate that the estimations provided by the models are in satisfying agreement with the simulation results.

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