

Unambiguous Representation for Sliceable Rectangular Floorplans

Soumya Pratik Saha^{#1}, Satrajit Ghosh^{*2}

^{#1} Department of Computer Science
West Bengal State University, Kolkata, India

^{*2} Department of Computer Science
Acharya Prafulla Chandra College, Kolkata, India

Abstract— Representation of a Rectangular Floorplan (RF) using Binary Expression Tree (BET) is a prevalent practice. Interestingly unique reconstruction of the Floorplan from BET poses a challenge because of the ambiguity involved in this representation. Unique encoding technique required for RF representation which overcomes the representational problem associated with reconstruction of RF from BET. A Topological Binary Tree (TBT) is proposed in this work whose structure itself defines the connectivity of the modules of RF so unique reconstruction of RF is possible from TBT .

Keywords— Rectangular Floorplan, Sliceable Floorplan, Adjacency graph, Geometric Duality, Baxter Number, Schroder Number, Floorplan Reconstruction, Binary Expression Tree, Topological Binary Tree.

I. INTRODUCTION

Floorplanning became an important phase of VLSI physical design due to increasing design complexity and circuit size of VLSI design. Floorplanning defines the topology of the layout, relative position of the modules and their interconnection to achieve optimal chip area, make routing phase easy and improve performance by reducing signal delays among modules [1]. Efficient Floorplan representation thus became an important issue as the performance criteria based on the geometrical representation of circuit blocks.

Interconnection between different functional modules in Floorplan represented by the graph called Adjacency Graph where Vertices represent Circuit/functional modules and edges represent their connectivity. A Floorplan and its Adjacency graph have a Geometric Duality relationship. Rectangular realisation of Adjacency Graph is called Rectangular Graph [10].

Efficient Floorplan representation must satisfy two important characteristics. First, representation must be unambiguous i.e. unique Floorplan generated from the Floorplan representation and second, transformation between representations to its corresponding Floorplan takes minimum time.

II. RECTANGULAR FLOORPLAN

A rectangular Floorplan is a non-overlapping rectangular dissection by horizontal and vertical T-junctions (F, ⊥, T, ⊢) line segments called cuts. Rectangular Floorplan is sliceable if it is obtained by recursively dividing a rectangle by horizontal and vertical cuts till the level of indivisible module otherwise called non-sliceable [1]. Two Floorplans

are said to be equivalent if and only if there is a one to one mapping between their set of blocks i.e. corresponding blocks lies in both Floorplan have the same relative position and it does not depends on the size of the block. In Mosaic Floorplan rectangular region divided into horizontal and vertical segments into rectangular region and each region corresponds to exactly one block. Two Mosaic Floorplans are said to be equivalent if and only if both Floorplan generate identical Horizontal Constraint graph (a Directed Graph defines the horizontal relationship between the vertical line segments of a Floorplan) and Vertical Constraint graph (a Directed Graph defines the vertical relationship between the horizontal line segments of a Floorplan) [11].

Theorem: The number of distinct Mosaic Floorplans with n blocks is equal to the nth Baxter Number B(n) [8]

$$B(n) = \binom{n+1}{C_1}^{-1} \binom{n+1}{C_2}^{-1} \sum_{k=1}^{n-1} \binom{n+1}{C_{k-1}} \binom{n+1}{C_k} \binom{n+1}{C_{k+1}}$$

Theorem: The number of Slicing Floorplans with n blocks where n>1 is equal to the twice the Schroder Number A_n defined by: [9]

$$A_0=1; A_1=1;$$

$$A_n = (3(2n-3) A_{n-1} - (n-3) A_{n-2}) / n;$$

III. BINARY TREE REPRESENTATION OF SLICEABLE FLOORPLAN

A sliceable Floorplan with n modules have in total (n-1) horizontal and vertical cut. Intersection of horizontal and vertical cut makes a T-cut junction (0° T-cut, 90° T-cut, 180° T-cut, 270° T-cut). There is one to many relationships between Sliceable Floorplan and its equivalent Binary Expression Tree having 2n-1 nodes with (n-1) internal node, n external node, obtained by recursively dividing a rectangular module by horizontal and vertical cut depicted in Fig. 1(a) and in Fig. 1(b)

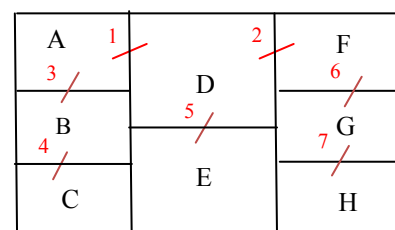


Fig. 1(a) Rectangular Sliceable Floorplan

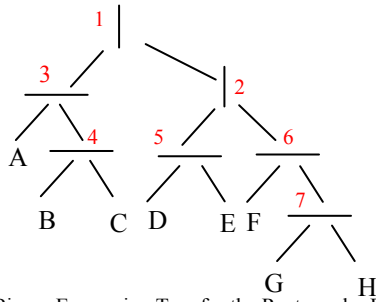


Fig. 1(b) Equivalent Binary Expression Tree for the Rectangular Floorplan shown in Fig. 1(a)

Compact representation of the above Floorplan is the post order traversal sequence of the binary expression tree. For the Binary Expression Tree of Fig. 1(b) equivalent post order traversal sequence is: A B C **h4 h3** D E **h5** F G H **h7 h6 v2 v1**

IV. PROPERTIES OF BINARY TREE REPRESENTS FLOORPLAN

- i. It is a rooted ordered tree, each internal node represent horizontal or vertical cut and external node represent rectangular module.
- ii. Floorplan with n modules represented by his tree having (n-1) internal node and n external node
- iii. Floorplan with n modules represented by his tree having (n-1) internal node and n external node
- iv. If H_i is a horizontal cut and A_i and B_i are two modules lies at the left and the right of the H_i then A_i became left child and B_i became the right child of H_i .
- v. If a rectangular module R_i contains the horizontal cut $h_0, h_1, h_2, \dots, h_{n-1}$ from top to bottom then slicing the module started from top i.e. h_0 to bottom i.e. h_{n-1} .
- vi. If a rectangular module R_i contains the vertical cut $v_0, v_1, v_2, \dots, v_{n-1}$ from top to bottom then slicing the module started from left i.e. v_0 to right i.e. v_{n-1} .

V. RECONSTRUCTION OF FLOORPLAN FROM BINARY TREE

There is one-to-many relationships between Binary tree and its generated Floorplan, for that reason during reconstruction of Floorplan from the binary expression tree generated Floorplans are not identical with the actual Floorplan shown in Fig. 1(a) because of the lack of information between module connectivity. The horizontal cut that separates D and E misplaced shown in Fig: 2(a) using dashed line. Due to this misplacement modules (C D) and (H D) became connected which are not connected in actual Floorplan. Similarly the horizontal cut that separates F and G misplaced in Fig. 2(b) has shown using dashed line.

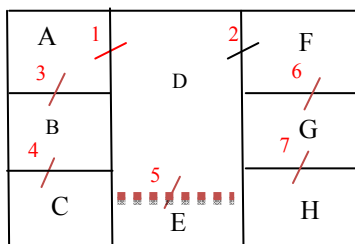


Fig. 2(a) Misplacement of **h5**

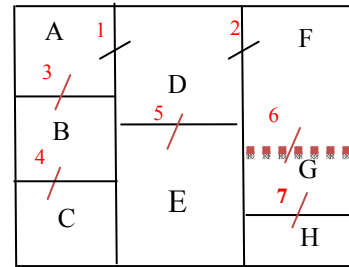


Fig. 2(b) Misplacement of **h6**

VI. REASON OF AMBIGUITY IN RECONSTRUCTION OF FLOORPLAN

If two horizontal cut incident on a vertical cut and one at the left and other right of the vertical cut or two vertical cut incident on a horizontal cut one at the top and other at the bottom of the horizontal cut then the information of their exact position cannot be obtained from the binary expression tree or from the post order traversal as a result different Floorplans are generated.

VII. UNIQUE RECONSTRUCTION OF FLOORPLAN USING TOPOLOGICAL BINARY TREE

In this work we propose a modified Binary tree representation for Sliceable Floorplan that encode the topological relationships of the modules and uniquely reconstruct it. Essential connectivity information of the Floorplan modules whose ignorance causes redundancy in reconstruction captured in this tree representation by formulating relationships between left most nodes of the sub trees.

Focusing on the portions of rectangular modules where horizontal cut incident on vertical cut and vertical cut incident on horizontal cut essential information's are obtained. Two sides of the vertical cut are checked from top to bottom and collect the information by checking the bottom part of every module.

If $L_1, L_2, L_3, \dots, L_m$ are the left side modules and $R_1, R_2, R_3, \dots, R_n$ are the Right side modules of the vertical cut V_i then in order to find out connectivity information either check left side modules or right side modules based on $\min(m, n)$.

Number of connectivity information $C_{\min} = \{\min(m, n) - 1\}$ as no need to store information of bottom most module of either side.

Illustrative Example:1

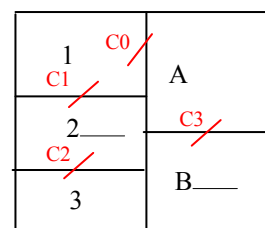


Fig. 3(a) Sliceable Rectangular Floorplan

Floorplan depicted in Fig. 3(a) left hand side of the vertical cut(C0) have three modules (1,2,3) and right hand side have two modules (A,B). Number of modules in left side > Number of modules in Right side

So right side module's connectivity are checked with the left side modules to optimize essential connectivity information.

Essential optimal connectivity information: (A 2)

This connectivity information together with its equivalent Binary Expression tree shown in Fig. 3(b) can reconstruct the Floorplan uniquely

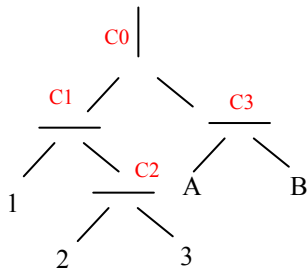


Fig. 3(b) Equivalent Binary Expression Tree for the Rectangular Floorplan depicted in Fig. 3(a)

In Topological Binary Tree Inorder predecessor of Left Subtree and Right Subtree represents essential connectivity as shown in Fig. 3(c)

Inorder predecessor (C3): A Inorder predecessor (C12*): 2

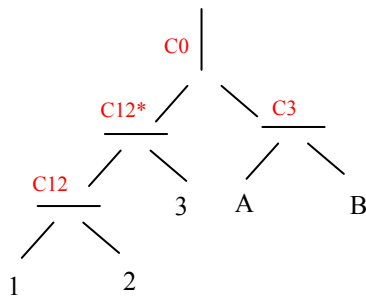


Fig. 3(c) Equivalent Topological Binary Tree for the Rectangular Floorplan depicted in Fig. 3(a)

Illustrative Example:2

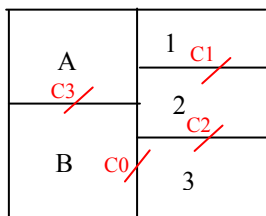


Fig. 4(a) Sliceable Floorplan

Floorplan depicted in Fig. 4(a) left hand side of the vertical cut(C0) have two modules (A,B) and right hand side have three modules (1,2,3)

Essential optimal connectivity information: (A 2)

This connectivity information together with its equivalent Binary Expression tree shown in Fig. 4(b) can reconstruct the Floorplan uniquely .

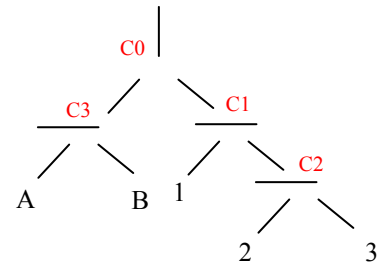


Fig. 4(b) Equivalent Binary Expression Tree for the Rectangular Floorplan depicted in Fig. 4(a)

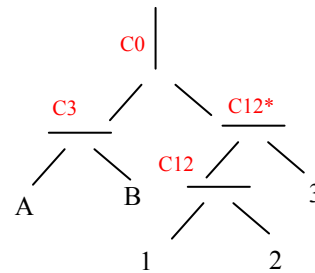


Fig. 4(c) Equivalent Topological Binary Tree for the Rectangular Floorplan depicted in Fig. 4(a)

In Topological Binary Tree Inorder predecessor of Left Subtree and Right Subtree represents essential connectivity as shown in Fig. 4(c)

Inorder predecessor (C3): A Inorder predecessor (C12*): 2

Illustrative Example:3

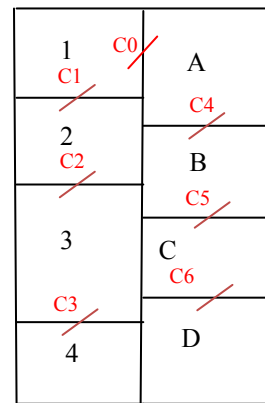


Fig. 5(a) Sliceable Rectangular Floorplan

Floorplan depicted in Fig. 5(a) left hand side of the vertical cut(C0) have four modules (1,2,3,4) and right hand side have also four modules (A,B,C,D).

Essential optimal connectivity information: (1 A)(2 B)(3 D)

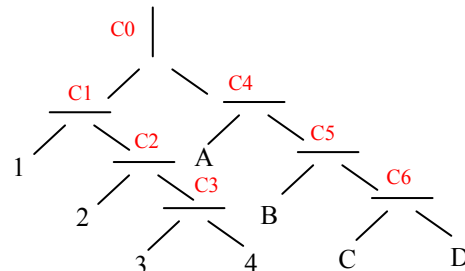


Fig. 5(b) Equivalent Binary Expression Tree for the Rectangular Floorplan depicted in Fig. 5(a)

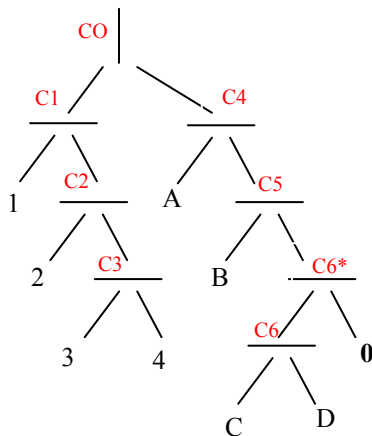


Fig. 5(c) Equivalent Topological Binary Tree for the Rectangular Floorplan depicted in Fig. 5(a)

This connectivity information together with its equivalent Binary Expression tree shown in Fig. 5(b) can reconstruct the Floorplan uniquely. In Topological Binary Tree Inorder predecessor of Left Subtree and Right Subtree represents essential connectivity as shown in Fig. 5(c). In this TBT extra leaf node is introduced labelled as 'o' for preserving consistency.

Inorder predecessor (C1): 1 Inorder predecessor (C4): A
 Inorder predecessor (C2): 2 Inorder predecessor (C5): B
 Inorder predecessor (C3): 3 Inorder predecessor (C6*): D

Illustrative Example :4

1	C0	A
	C1	C4
2		B
	C2	C5
		C
		C6
3		D
		C7
		E
4		C8
		F

Fig. 6(a) Sliceable Rectangular Floorplan

Floorplan depicted in Fig. 6(a) left hand side of the vertical cut(C0) have four modules (1,2,3,4) and right hand side have six modules (A,B,C,D,E,F). Therefore, Number of modules in left side < Number of modules in Right side
 So left side module's connectivity checked with the right side modules.
 Essential optimal connectivity information: (1 B)(2 C)(3 E)
 This connectivity information together with its equivalent Binary Expression tree shown in Fig. 6(b) can reconstruct the Floorplan uniquely

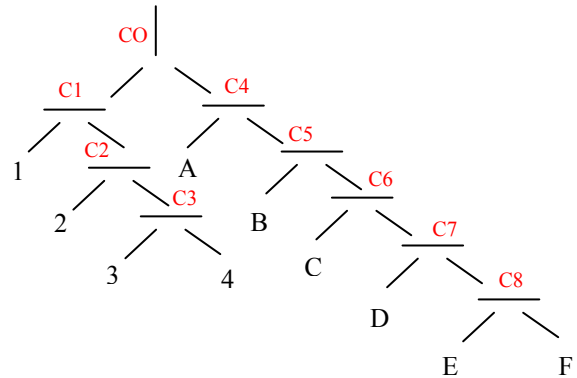


Fig. 6(b) Equivalent Binary Expression Tree for the Rectangular Floorplan depicted in Fig. 6(a)

In Topological Binary Tree Inorder predecessor of Left Subtree and Right Subtree represents essential connectivity as shown in Fig. 6(c)

Inorder predecessor (C1): 1 Inorder predecessor (C45*): B
 Inorder predecessor(C2): 2 Inorder predecessor (C6):C
 Inorder predecessor (C3): 3 Inorder predecessor (C78*): E

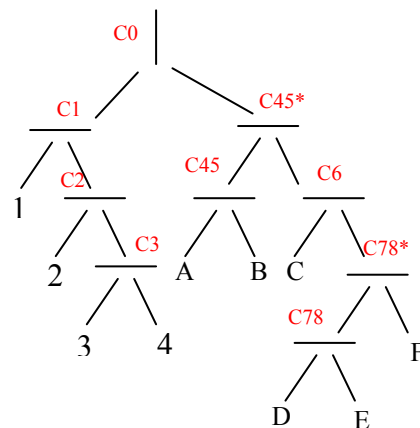


Fig. 6(c) Equivalent Topological Binary Tree for the Rectangular Floorplan depicted in Fig. 6(a)

VIII. CONCLUSIONS

An exhaustive study has done to find out number of Binary Expression Tree possible with *n* internal nodes labelled with vertical and horizontal cuts that generate ambiguous Floorplan. If a Binary Expression Tree has symmetry with another tree then both generate same Floorplan layout with different orientation of rectangles. Proposed work performs exhaustive search to identify the reason behind the ambiguity and explores the possible solutions to solve the problem. It is found that there exist a large number of expression trees from which unique reconstruction is possible and ambiguity can be avoided if the essential connectivity information of modules maintained with the Binary Expression Tree. Proposed work combine essential requirements(BET and extra information of module connectivity) used for unique reconstruction of Floorplan and mapped it into a single tree'Topological Binary Tree'.

Formation of efficient Algorithm for the construction of Topological Binary Tree, optimization of internal nodes and removal of Empty leaf nodes are proposed in future.

REFERENCES

- [1] P. Dasgupta and S Sur-kolay., *Sliceable Rectangular Graphs and Their optimal Floorplans*, ACM Transactions on Design Automation of Electronic Systems ,vol. 6,No.4,October 2001,pages 447-470.
- [2] B.Yao, H.Chen,C. Cheng, R. Graham, "*Floorplan Representations: Complexity and Connections* " in ACM Transactions on Design Automation of Electronic Systems,Vol. 8,No.1,January 2003, pages 55-80
- [3] N. Sherwani, "*Algorithm for VLSI Physical Design Automation*", Third Edition, Springer International Edition.
- [4] T. Izumi, A. Takahashi , and Y. Kajitani ,"*Fast Algorithms for General Floorplan*", Published in IEEE Design Automation Conference 1998. Proceedings of the ASP-DAC '98. Asia and South Pacific.
- [5] M. Sarrafzadeh and C. K. Wong, "*An Introduction to VLSI Physical Design*", McGraw-Hill International editions, International edition 1996
- [6] P. S. Dasgupta, S. Sur-Kolay, and B. B. Bhattacharya, "A unified approach to topology generation and optimal sizing of floorplans," *IEEE Trans.*, vol. 17, pp. 126–135, Feb. 1998. .
- [7] P. Banerjee, S Sur-kolay, A Bishnu , "*Fast Unified Floorplan Topology Generation and Sizing on Heterogeneous Field-programmable gate-arrays* ", in IEEE Trans. On Computer Aided Design of Integrated Circuits and Systems, vol.28,no.5,May 2009,pp.651-661
- [8] G. Baxter, on "*Fixed Points of the composite of Commuting Functions*", Proc. Amer. Math. Soc.15 ,6,851-855 on 1964.
- [9] Etherington, I.M.H, Some problems of non-associative Combinations, Edinburgh Math ,Notes 32, pp i-vi
- [10] K. Kozminski and K. Kinnen ,"*Rectangular Duals of Planar Graphs*" Networks 15, 2, 145-157
- [11] Xianlong Hong, Gang Huang, Yici Cai, Jiangchun Gu, Sheqin Dong, Chung-Kuan Cheng,and Jun Gu. Corner-block list: An effective and efficient topological representation of non-slicing floorplan. In *Proceedings of the International Conference on Computer Aided Design,(ICCAD'00)*, pages 8–12, 2000.